HETEROSTRUCTURE BIPOLAR TRANSISTOR POWER AMPLIFIER MODULE WITH DYNAMIC VOLTAGE SUPPLY FOR IMPROVED EFFICIENCY

Cross-reference to Related Applications

[0001] This application claims the benefit of U.S. Provisional Application No. 60/456,423, filed March 19, 2003, which is incorporated herein by reference.

BACKGROUND

[0002] The invention relates to a heterostructure bipolar transistor power amplifier module, and more particularly to a power amplifier module with a dynamic voltage supply.

[0003] As the wireless industry for handheld phones matures, it is insufficient for a power amplifier module (PAM) to meet a specification at a low cost, and with a small footprint while accepting whatever power efficiency at power back-off occurs once the efficiency is optimized at maximum power. The power efficiency drops dramatically with lower output power due to the impedance mismatch between the constant low impedance output match and the rising impedance of the output stage. This is of particular importance with Code Division Multiple Access (CDMA) technology, because in CDMA the probability of the output power is the greatest between 12 to 18 dB power back-off from a nominal maximum and falls to a minimum at either a maximum or minimum power limit.

[0004] A simple yet popular approach for improving power efficiency in the power back-off high probable area is to change the 'mode' of operation of the amplifier. By moving the 'mode of operation' to more of a class B amplifier from a class A amplifier, the efficiency improves. This is achieved by lowering the quiescent current through the RF stages using a simple switch in the DC bias circuitry. The amplifier is switched between states or modes at a 8 to 12 dB back-off, and the efficiency improvement is typically a few percent.

[0005] Another approach is to use a DC-DC converter for the main power supply for the power amplifier. Reducing the collector supply voltage(s) when the PAM output requirement is at a lower power level can result in a much higher efficiency improvement, by 100 to 300% (depending on the power level), because the output transistor impedance stays relatively constant with lower power as the supply voltage is also lowered. However, for most HBT amplifiers, this

approach only works in the collector voltage range of 4 Volts down to about 1.5 Volts. At best, the output stage collector voltage (Vcc2 for a two stage amplifier) may be reduced to below 1.5 Volts. This limits the useful dynamic output power range to about 10 dB.

[0006] Figure 1 shows the probability distribution function of the transmission power of handheld phone for CDMA for urban areas and a data mode. It can be seen that PAM works only 4% of the time in its enhanced efficiency state whereas the PAM works about 17% of the time in the data mode.

SUMMARY

[0007] A power amplifier module includes first and second RF stages and first and second bias circuits for the first and second RF stages, respectively. Power is supplied to the bias circuits separately from the power supplied to the first and second RF stages.

[0008] In one aspect, the first and second RF stages are powered by first and second voltages Vcc1 and Vcc2, respectively. A voltage Vref sets a bias point of the first and second bias circuits. A voltage Vcb powers the first and second bias circuits. The voltage Vcb is provided to the power amplifier module separately from the first and second voltages Vcc1 and Vcc2.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is a graph illustrating an output power probability distribution function for urban usage and for a data transmission mode for a CDMA system.

[0010] Figure 2 is a schematic diagram illustrating a conventional power amplifier module bias circuit.

[0011] Figure 3 is a top plan view illustrating a conventional 4 millimeter by 4 millimeter power amplifier module package and pinout.

[0012] Figure 4 is a schematic diagram illustrating a power amplifier module bias circuit.

[0013] Figure 5 is a top plan view illustrating a power amplifier module package and pinout for the circuit of Figure 4.

[0014] Figure 6 is a schematic illustrating a power amplifier module including an emitter resistor and a base resistor.

DETAILED DESCRIPTION

[0015] To take full advantage of the DC-DC switching supply voltage for CDMA applications, the power amplifier module of the present invention may operate over a supply voltage range that equates to a 20 to 25 dB power range. With this range, the power amplifier module operates at high efficiency 28% of the time for urban areas and at about 65% of the time for a data mode. In one embodiment, the power amplifier module should operate down to approximately 0.5 Volt supply to achieve this dynamic range for high efficiency.

[0016] Figure 2 is a schematic diagram illustrating a conventional power amplifier module bias circuit 200.

[0017] The power amplifier module 200 comprises a plurality of transistors 201 through 206, a plurality of resistors 208 and 209, a plurality of inductors 212 through 215, and a plurality of capacitors 218 through 221. A first stage of the power amplifier 200 includes the transistor 206, the inductor 213, and the capacitor 219. A bias circuit for the first stage of the power amplifier 200 include the transistors 201 and 202, the resistor 208, and the inductor 212. A second stage of the power amplifier 200 includes the transistor 205, the inductor 215, and the capacitor 221. A bias circuit for the second stage of the power amplifier 200 include the transistors 203 and 204, the resistor 209, and the inductor 214.

[0018] Figure 3 is a top plan view illustrating the package and pinout of the power amplifier module 200.

[0019] Three separate voltages set the bias or operating condition amplifier. A voltage Vcc1 sets the voltage of the first stage. A voltage Vcc2 sets the voltage of the second stage. A reference voltage Vref sets voltage of the bias circuits and thus sets the quiescent current of the

amplifier. Each voltage is controlled separately from a corresponding pin in the module as shown in Figure 3.

[0020] The bias circuitry of the HBT PAM 200 includes a voltage Vcb being coupled to the voltage Vcc of the first stage (Vcc1). When the HBT PAM 200 operates at low collector voltages (Vcc1 and Vcc2), the bias supply adversely affects the RF operation if the voltage Vcb falls below about 1.4 volts. The voltage Vcb is the voltage level at the collectors of the transistors 202 and 204. Coupling the voltage Vcb to the voltage Vcc of the first stage (Vcc1), as shown in Figure 2, is done to match the industry standard PAM pin configuration shown in Fig 3.

[0021] Figure 4 is a schematic diagram illustrating a power amplifier module bias circuit 400. Figure 5 is a top plan view of the package and pinout of the power amplifier module 400.

[0022] The power amplifier module 400 comprises a plurality of transistors 401 through 406, a plurality of resistors 408 and 409, a plurality of inductors 412 through 415, and a plurality of capacitors 418 through 421. A first stage of the power amplifier 400 includes the transistor 406, the inductor 413, and the capacitor 419. A bias circuit for the first stage of the power amplifier 400 include the transistors 401 and 402, the resistor 408, and the inductor 412. A second stage of the power amplifier 400 includes the transistor 405, the inductor 415, and the capacitor 421. A bias circuit for the second stage of the power amplifier 400 include the transistors 403 and 404, the resistor 409, and the inductor 414.

[0023] Four separate voltages set the bias or operating condition amplifier. A voltage Vcc1 sets the voltage of the first stage. A voltage Vcc2 sets the voltage of the second stage. A reference voltage Vref sets voltage of the bias circuits and thus sets the quiescent current of the amplifier. A voltage Vcb sets the voltage of the bias circuits. Each voltage is controlled separately from a corresponding pin in the module as shown in Figure 5.

[0024] The power amplifier 400 is similar to the power amplifier 200 with the elements 401 through 421 being similarly connected as elements 201 through 221, except for the connection of the collectors of the transistors 402 and 404. In the power amplifier module 200, the collectors

of the transistors 202 and 204 are coupled together and to the voltage source Vcc1. In the power amplifier 400, the collectors of the transistors 402 and 404 are coupled to the voltage Vcb. The pinout of the power amplifier module 400 has been modified so that a "spare" ground pad (main ground is the center island) of the power amplifier 200 shown in Figure 3 now couples to the voltage Vcb as shown in Figure 5. In the arrangement of the power amplifier module 400, the voltage Vcb is held at 2.5 volts or higher, such as the battery voltage, and the voltages Vcc1 and Vcc2 are controlled down to a voltage of 0.5 volts.

[0025] In another embodiment, the voltage Vcb can be connected to the Vref terminal, which, for example, may be kept at a voltage of 2.7V or higher at all times. In this configuration, a pin configuration that is the same as shown in Figure 3 may be used with the new bias circuitry with this invention, provided that the total current at Vref terminal meets system specification. This embodiments allows a package pin configuration to remain constant, but with different connections inside the package.

[0026] Figure 6 is a schematic diagram illustrating a power amplifier module 600 including an emitter resistor and a base resistor.

[0027] A power amplifier 600 comprises a plurality of transistors 601 through 603, a plurality of resistors 606 through 608, a plurality of inductors 610 and 611, and a plurality of capacitors 614 and 615. The power amplifier 600 may further comprise a plurality of parallel transistor fingers that each include a transistor 603, an inductor 611, a capacitor 614, and a resistor 608 coupled together in parallel.

[0028] Another area that will limit low voltage operation is in using emitter ballast resistors for ensuring proper current sharing among all the parallel transistor fingers. The emitter resistor 608 also has a voltage drop and thus limits the lowest voltage that can be applied to the collector of the transistor 603 and still maintain proper linear operation.

[0029] In one embodiment, the emitter resistor 608 is removed (or has a zero resistance). By using the base resistor 607 instead of the emitter resistor 608, the base resistor 607 also allows

proper current sharing of the parallel transistors but is not in line with the collector current and allows all the supply voltage across the RF transistor 603.